AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1. (original) A semiconductor memory device comprising:

a memory cell having a first transfer MISFET and a second transfer MISFET disposed at portions where a pair of complementary data lines and a word line intersect, a first drive MISFET and a second drive MISFET, and a first vertical MISFET and a second vertical MISFET, the first drive MISFET and the first vertical MISFET, and the second drive MISFET and the second vertical MISFET being cross-connected,

wherein the first and second transfer MISFETs, and the first and second drive MISFETs are formed on a major surface of a semiconductor substrate,

wherein the first and second vertical MISFETs are formed over the first and second transfer MISFETs and the first and second drive MISFETs respectively,

wherein the first vertical MISFET has a source, a channel region and a drain formed in a first laminated body extending in a direction perpendicular to the major surface of the semiconductor substrate, and a gate electrode formed on sidewall portions of the first laminated body with a gate insulating film interposed therebetween,

wherein the second vertical MISFET has a source, a channel region and a drain of a second laminated body extending in a direction perpendicular to the major surface of the semiconductor substrate, and a gate electrode formed on sidewall portions of the second laminated body with a gate insulating film interposed therebetween, and

wherein the sources of the first and second vertical MISFETs are electrically connected to a source voltage line formed over the first and second laminated bodies.

2. (original) The semiconductor memory device according to claim 1, wherein one of the complementary data lines, which is electrically connected to one of a source and drain of the first transfer MISFET, and the other of the complementary data lines, which is electrically connected to one of a source and drain of the second transfer MISFET, are formed in the same wiring layer as the source voltage line.

3. (original) The semiconductor memory device according to claim 1, wherein the word line electrically connected to gate electrodes of the first and second transfer MISFETs is formed in a wiring layer above the source voltage line and the complementary data lines.

4. (original) The semiconductor memory device according to claim 1, wherein reference voltage lines electrically connected to sources of the first and second drive MISFETs are formed in the same wiring layer as the word line.

5. (original) The semiconductor memory device according to claim 1, wherein the reference voltage lines comprise a first reference voltage line electrically connected to the source of the first drive MISFET, and a second reference voltage line electrically connected to the source of the second drive MISFET, and the first reference voltage line and the second reference voltage line extend in a first direction with the word line being arranged therebetween.

6. (original) The semiconductor memory device according to claim 5, wherein one of the complementary data lines and the other thereof extend in a second direction intersecting the first direction with the source voltage line being interposed therebetween.

7. (original) The semiconductor memory device according to claim 1, wherein the complementary data lines, the source voltage line, the reference voltage lines and the word line are constituted of a metal film comprised of copper as a principal component.

8. (original) A semiconductor memory device comprising:

a memory cell having a first transfer MISFET and a second transfer MISFET disposed at portions where a pair of complementary data lines and a word line intersect, a first drive MISFET and a second drive MISFET, and a first vertical MISFET and a second vertical MISFET, the first drive MISFET and the first vertical MISFET, and the second drive MISFET and the second vertical MISFET being cross-connected,

wherein the first and second transfer MISFETs, and the first and second drive MISFETs are formed on a major surface of a semiconductor substrate,

wherein the first vertical MISFET is disposed on one end of a gate electrode of the second drive MISFET and has a source, a channel region and a drain formed in a first laminated body extending in a direction perpendicular to the major surface of the semiconductor substrate, and a gate electrode formed on sidewall portions of the first laminated body with a gate insulating film interposed therebetween, and

wherein the second vertical MISFET is disposed on one end of a gate electrode of the first drive MISFET and has a source, a channel region and a drain formed in a second laminated body extending in a direction perpendicular to the major surface of the semiconductor substrate, and a gate electrode formed on sidewall portions of the second laminated body with a gate insulating film interposed therebetween.

9. (original) The semiconductor memory device according to claim 8, wherein the first and second vertical MISFETs are disposed between areas for forming the first transfer MISFET and the first drive MISFET and areas for forming the second transfer MISFET and the second drive MISFET as viewed on a plane basis in a plane parallel to the major surface of the semiconductor substrate.

10. (original) A semiconductor memory device comprising:

a memory cell having a first transfer MISFET and a second transfer MISFET disposed at portions where a pair of complementary data lines and a word line intersect, a first drive MISFET and a second drive MISFET, and a first vertical MISFET and a second vertical MISFET, the first drive MISFET and the first vertical MISFET, and the second drive MISFET and the second vertical MISFET being cross-connected,

wherein the first and second transfer MISFETs, and the first and second drive MISFETs are formed on a major surface of a semiconductor substrate,

wherein the first and second vertical MISFETs are formed over the first and second transfer MISFETs and the first and second drive MISFETs,

wherein the first vertical MISFET has a source, a channel region and a drain formed in a first laminated body extending in a direction perpendicular to the major surface of the semiconductor substrate, and a first gate electrode formed on sidewall portions of the first laminated body with a gate insulating film interposed therebetween,

wherein the second vertical MISFET includes a source, a channel region and a drain formed in a second laminated body extending in a direction perpendicular to the major surface of the semiconductor substrate, and a second gate electrode formed on sidewall portions of the second laminated body with a gate insulating film interposed therebetween,

wherein the drain of the first vertical MISFET, a gate electrode of the second drive MISFET, and a drain of the first drive MISFET are electrically connected to one another through a first intermediate conductive layer,

wherein the drain of the second vertical MISFET, a gate electrode of the first drive MISFET, and a drain of the second drive MISFET are electrically connected to one another through a second intermediate conductive layer,

wherein the first gate electrode of the first vertical MISFET is electrically connected to the second intermediate conductive layer through a first gate drawing electrode formed so as to come into contact with the first gate electrode, and a first conductive layer lying in a first connecting hole and formed so as to come into contact with the first gate drawing electrode and the second intermediate conductive layer, and

wherein the second gate electrode of the second vertical MISFET is electrically connected to the first intermediate conductive layer through a second gate drawing electrode formed so as to come into contact with the second gate electrode, and a second conductive layer lying in a second connecting hole and formed so as to come into contact with the second gate drawing electrode and the first intermediate conductive layer.

11. (original) The semiconductor memory device according to claim 10, wherein a plurality of MISFETs for each peripheral circuit are further formed on the major surface of the semiconductor substrate, and wirings for connecting between the MISFETs of the peripheral circuit and the first and second intermediate conductive layers are formed in the same wiring layer.

12. (original) The semiconductor memory device according to claim 10, wherein the first and second intermediate conductive layers are comprised of a metal film, a first barrier layer is formed between the drain of the first vertical MISFET and the first intermediate conductive layer, and a second barrier layer is formed between the drain of the second vertical MISFET and the second intermediate conductive layer.

13. (original) The semiconductor memory device according to claim 12, wherein the first and second intermediate conductive layers are constituted of a tungsten film, and the first and second barrier layers comprise a tungsten nitride (WN) film.

14. (original) The semiconductor memory device according to claim 10, wherein the first and second intermediate conductive layers are constituted of an oxidation resistant conductive film.

15. (original) The semiconductor memory device according to claim 10, wherein the first gate electrode of the first vertical MISFET is electrically connected to the first gate drawing electrode at a lower end thereof, and the second gate electrode of the second vertical MISFET is electrically connected to the second gate drawing electrode at a lower end thereof.

16. (original) The semiconductor memory device according to claim 10, wherein the first gate electrode of the first vertical MISFET and the second gate electrode of the second vertical MISFET are respectively comprised of two-layer conductive films.

17. (original) The semiconductor memory device according to claim 10, wherein the second intermediate conductive layer, the first gate drawing electrode and the first connecting hole are disposed so as to have portions which overlap each other on a plane basis, whereas the first intermediate conductive layer, the second gate drawing electrode and the second connecting hole are disposed so as to have portions which overlap each other on a plane basis.

18. (original) The semiconductor memory device according to claim 10, wherein the first connecting hole extends through the first gate drawing electrode to connect to the second intermediate conductive layer, and the second connecting hole extends through the second gate drawing electrode to connect to the first intermediate conductive layer.

19. (original) The semiconductor memory device according to claim 10, wherein the first gate drawing electrode is brought into contact with the first gate electrode of the first vertical MISFET at the sidewall portions of the first laminated body, and the second gate drawing electrode is brought into contact with the second gate electrode of the second vertical MISFET at the sidewall portions of the second laminated body.

20. (original) The semiconductor memory device according to claim 10, wherein the first gate drawing electrode is formed integrally with the first gate electrode of the first vertical MISFET, and the second gate drawing electrode is formed integrally with the second gate electrode of the second vertical MISFET.

21. (original) The semiconductor memory device according to claim 10, wherein the gate electrode of the first vertical MISFET is formed so as to surround the sidewall portions of the first laminated body, and the gate electrode of the second vertical MISFET is formed so as to surround the sidewall portions of the second laminated body.

22. (original) The semiconductor memory device according to claim 10, wherein each of the first and second gate drawing electrodes is comprised of a silicon conductive film and a silicide film formed on the surface thereof.

23. (original) The semiconductor memory device according to claim 1, wherein the first and second transfer MISFETs, and the first and second drive MISFETs comprise n channel type MISFETs respectively, and the first and second vertical MISFETs comprise p channel type MISFETs respectively.

Claims 24-29. (Canceled without prejudice or disclaimer).

Claims 30-31. (Canceled without prejudice or disclaimer).

Claim 32. (Canceled without prejudice or disclaimer).

33. (original) A semiconductor memory device comprising:

a memory cell which includes a first drive MISFET and a second drive MISFET and a first vertical MISFET and a second vertical MISFET, the first drive MISFET and the first vertical MISFET, and the second drive MISFET and the second vertical MISFET being cross-connected,

wherein the drive MISFETs are formed on a major surface of a semiconductor substrate, and

wherein gates of the vertical MISFETs formed over the drive MISFETs with an insulating film interposed therebetween are electrically connected to lower conductive films at lower portions thereof and thereby electrically connected to gates or drains of the drive MISFETs.

34. (original) A semiconductor memory device comprising:

a memory cell which includes a first drive MISFET and a second drive MISFET and a first vertical MISFET and a second vertical MISFET, the first drive MISFET and the first vertical MISFET, and the second drive MISFET and the second vertical MISFET being cross-connected,

wherein the drive MISFETs are formed on a major surface of a semiconductor substrate,

wherein the vertical MISFETs are respectively formed over the drive MISFETs with an insulating film interposed therebetween, and

wherein current paths between gates or drains of the drive MISFETs and gates of the vertical MISFETs are formed via lower portions of the gates of the vertical MISFETs through conductive films.

35. (original) A semiconductor memory device comprising:

a memory cell which includes a first drive MISFET and a second drive MISFET and a first vertical MISFET and a second vertical MISFET, the first drive MISFET and the first vertical MISFET, and the second drive MISFET and the second vertical MISFET being cross-connected,

wherein the drive MISFETs are formed on a major surface of a semiconductor substrate,

wherein conductive films electrically connected to gates or drains of the drive MISFETs are respectively formed over the drive MISFETs with an insulating film interposed therebetween,

wherein the vertical MISFETs are formed over the conductive films, and

wherein gate electrodes of the vertical MISFETs are shaped in the form of sidewall spacers and electrically connected to the conductive films.

36. (original) A semiconductor memory device comprising:

a memory cell which includes a first drive MISFET and a second drive MISFET and a first vertical MISFET and a second vertical MISFET, the first drive MISFET and the first vertical MISFET, and the second drive MISFET and the second vertical MISFET being cross-connected,

wherein the drive MISFETs are formed on a major surface of a semiconductor substrate,

wherein conductive films electrically connected to gate electrodes or drains of the drive MISFETs are formed over the drive MISFETs with an insulating film interposed therebetween,

wherein the vertical MISFETs are formed over the conductive films, and

wherein gate electrodes of the vertical MISFETs are electrically connected to the conductive films in a self-alignment manner.

37. (original) The semiconductor memory device according to claim 33,

wherein the vertical MISFETs are formed over the conductive films with an insulating film interposed therebetween,

wherein the gate electrodes of the vertical MISFETs respectively include a first film and a second film shaped in the form of sidewall spacers,

wherein the conductive film is opened in a self-alignment with the first film, and

wherein the second film is electrically connected to the corresponding conductive film.

38. (original) A semiconductor memory device comprising:

a memory cell which includes a first drive MISFET and a second drive MISFET and a first vertical MISFET and a second vertical MISFET, the first drive MISFET and the first vertical MISFET, and the second drive MISFET and the second vertical MISFET being cross-connected,

wherein the drive MISFETs are formed on a major surface of a semiconductor substrate,

wherein a first conductive film electrically connected to a gate or drain of each of the drive MISFETs is formed over the corresponding drive MISFET with an insulating film interposed therebetween,

wherein a second conductive film is formed over the first conductive film,

wherein each of the vertical MISFETs is formed over the second conductive film,

wherein a gate of the corresponding vertical MISFET is electrically connected to the second conductive film, and

wherein a drain of the corresponding vertical MISFET is electrically connected to the first conductive film not through the second conductive film.

39. (original) The semiconductor memory device according to claim 38,

wherein each of the vertical MISFETs is formed over the second conductive film with an insulating film interposed therebetween,

wherein the gates of the vertical MISFETs respectively include a first film and a second film shaped in the form of sidewall spacers,

wherein the second conductive film is opened in a self-alignment with the first film, and

wherein the second film is electrically connected to the second conductive film.

40. (original) The semiconductor memory device according to claim 38,

wherein the first conductive film is comprised of a metal film,

wherein the second conductive film is comprised of a silicon film, and

wherein the first conductive film is electrically connected to the drain of each of the vertical MISFETs via a barrier film.

41. (original) The semiconductor memory device according to claim 38, wherein conductive films, which are conductive films lying in the same layer as the first conductive film for electrical connection between gates and drains of MISFETs for each peripheral circuit, are formed.

42. (original) A semiconductor memory device comprising:

a memory cell having a first drive MISFET and a second drive MISFET and a first vertical MISFET and a second vertical MISFET; and

MISFETs for a peripheral circuit,

wherein the drive MISFETs are formed on a major surface of a semiconductor substrate,

wherein conductive films for electrical connection between gates and drains of the drive MISFETs, are formed over the drive MISFETs with an insulating film interposed therebetween,

wherein the vertical MISFETs are formed over the conductive films, and

wherein conductive films, which are conductive films lying in the same layer as said conductive films and carry out electrical connection between gates and drains of the MISFETs for the peripheral circuit, are formed.

43. (original) The semiconductor memory device according to claim 42,

wherein the conductive films are respectively constituted of a metal film, and

wherein the conductive films are electrically connected to drains of the vertical MISFETs via barrier films.

44. (original) The semiconductor memory device according to claim 42,

wherein a metal wiring layer is formed through an insulating film which covers the vertical MISFETs, and

wherein wirings for electrical connection between the gates and drains of the MISFETs for the peripheral circuit are formed by the metal wiring layer.

45. (original) A semiconductor memory device comprising:

a memory cell having a first drive MISFET and a second drive MISFET and a first vertical MISFET and a second vertical MISFET,

wherein the drive MISFETs are formed on a major surface of a semiconductor substrate,

wherein conductive films electrically connected to gates or drains of the drive MISFETs are formed over the drive MISFETs with an insulating film interposed therebetween,

wherein the vertical MISFETs are formed over the conductive films, and

wherein the conductive films and gate electrodes of the vertical MISFETs are respectively electrically connected by plugs embedded in connecting holes formed in an insulating film covering the vertical MISFETs.

46. (original) The semiconductor memory device according to claim 45, wherein conductive films, which are conductive films lying in the same layer as said conductive films for electrical connection between gates and drains of MISFETs for a peripheral circuit, are formed.

47. (original) The semiconductor memory device according to claim 30,

wherein each of the vertical MISFETs has a source, a channel region and a drain formed in a laminated body extending in a direction perpendicular to the major

surface of the semiconductor substrate, and a gate electrode formed on sidewall portions of the laminated body with a gate insulating film interposed therebetween, and

wherein the laminated body is comprised of a silicon film.

Claims 48-50. (Canceled without prejudice or disclaimer).

51. (original) The semiconductor memory device according to claim 10, wherein the first and second gate drawing electrodes are respectively comprised of a metal nitride film.

52. (original) The semiconductor memory device according to claim 16, wherein the first and second gate drawing electrodes are respectively comprised of a metal nitride film, and the conductive film brought into contact with the first gate drawing electrode, of the two-layer conductive films constituting the first gate electrode of the first vertical MISFET, and the conductive film brought into contact with the second gate drawing electrode, of the two-layer conductive films constituting the second gate electrode of the second vertical MISFET are respectively comprised of a metal film.

53. (original) The semiconductor memory device according to claim 12, wherein the drain of the first vertical MISFET is electrically connected to the first barrier layer through a first plug formed of a silicon film,

wherein the drain of the second vertical MISFET is electrically connected to the second barrier layer through a second plug formed of a silicon film,

wherein a first reactive layer for preventing a reaction between the first plug and the first barrier layer is formed therebetween, and

wherein a second reactive layer for preventing a reaction between the second plug and the second barrier layer is formed therebetween.

54. (original) The semiconductor memory device according to claim 53, wherein depressions and projections are provided on the surfaces of the first and second reactive layers.

55. (original) The semiconductor memory device according to claim 53, wherein the silicon film constituting each of the first and second plugs is one formed by annealing an amorphous silicon film deposited by a CVD method using a source gas containing disilane.

Claims 56-68. (Canceled without prejudice or disclaimer).

69. (Previously Presented) A semiconductor memory device comprising:

a memory cell which includes a first drive MISFET and a second drive MISFET and a first vertical MISFET and a second vertical MISFET, the first drive

MISFET and the first vertical MISFET, and the second drive MISFET and the second vertical MISFET being cross-connected,

wherein the drive MISFETs are formed on a major surface of a semiconductor substrate,

wherein a metal film for cross-connecting gates and drains of the first and second drive MISFETs is formed over the drive MISFETs with an insulating film interposed therebetween, and

wherein the vertical MISFETs connected to the metal film are formed over the metal film,

wherein the vertical MISFETs are formed over the metal film with an insulating film interposed therebetween,

wherein the gate electrodes of the vertical MISFETs respectively include a first film and a second film shaped in the form of sidewall spaces,

wherein the metal film is opened in a self-alignment with the first film, and

wherein the second film is electrically connected to the corresponding conductive film.

70. (Previously Presented) A semiconductor memory device comprising:

a memory cell which includes a first drive MISFET and a second drive MISFET and a first vertical MISFET and a second vertical MISFET, the first drive MISFET and the first vertical MISFET, and the second drive MISFET and the second vertical MISFET being cross-connected,

wherein the drive MISFETs are formed on a major surface of a semiconductor substrate, and

wherein gates of the vertical MISFETs formed over the drive MISFETs with an insulating film interposed therebetween are electrically connected to lower conductive films at lower portions thereof and thereby electrically connected to gates or drains of the drive MISFETs,

wherein the vertical MISFETs are formed over the conductive films with an insulating film interposed therebetween,

wherein the gate electrodes of the vertical MISFETs respectively include a first film and a second film shaped in the form of sidewall spaces,

wherein the metal film is opened in a self-alignment with the first film, and

wherein the second film is electrically connected to the corresponding conductive film.

71. (Previously Presented) A semiconductor memory device comprising:

a memory cell which includes a first drive MISFET and a second drive MISFET and a first vertical MISFET and a second vertical MISFET, the first drive MISFET and the first vertical MISFET, and the second drive MISFET and the second vertical MISFET being cross-connected,

wherein the drive MISFETs are formed on a major surface of a semiconductor substrate,

wherein the vertical MISFETs are respectively formed over the drive MISFETs with an insulating film interposed therebetween,

wherein current paths between gates or drains of the drive MISFETs and gates of the vertical MISFETs are formed via lower portions of the gates of the vertical MISFETs through conductive films,

wherein the vertical MISFETs are formed over the conductive films with an insulating film interposed therebetween,

wherein the gate electrodes of the vertical MISFETs respectively include a first film and a second film shaped in the form of sidewall spaces,

wherein the metal film is opened in a self-alignment with the first film, and

wherein the second film is electrically connected to the corresponding conductive film.

72. (Previously Presented) A semiconductor memory device comprising:

a memory cell which includes a first drive MISFET and a second drive MISFET and a first vertical MISFET and a second vertical MISFET, the first drive MISFET and the first vertical MISFET, and the second drive MISFET and the second vertical MISFET being cross-connected,

wherein the drive MISFETs are formed on a major surface of a semiconductor substrate,

wherein conductive films electrically connected to gates or drains of the drive MISFETs are respectively formed over the drive MISFETs with an insulating film interposed therebetween,

wherein the vertical MISFETs are formed over the conductive films,

wherein gate electrodes of the vertical MISFETs are shaped in the form of sidewall spacers and electrically connected to the conductive films,

wherein the vertical MISFETs are formed over the conductive films with an insulating film interposed therebetween,

wherein the gate electrodes of the vertical MISFETs respectively include a first film and a second film shaped in the form of sidewall spaces,

wherein the metal film is opened in a self-alignment with the first film, and

wherein the second film is electrically connected to the corresponding conductive film.

73. (Previously Presented) A semiconductor memory device comprising:

a memory cell which includes a first drive MISFET and a second drive MISFET and a first vertical MISFET and a second vertical MISFET, the first drive MISFET and the first vertical MISFET, and the second drive MISFET and the second vertical MISFET being cross-connected,

wherein the drive MISFETs are formed on a major surface of a semiconductor substrate,

wherein conductive films electrically connected to gate electrodes or drains of the drive MISFETs are formed over the drive MISFETs with an insulating film interposed therebetween,

wherein the vertical MISFETs are formed over the conductive films,

wherein gate electrodes of the vertical MISFETs are electrically connected to the conductive films in a self-alignment manner,

wherein the vertical MISFETs are formed over the conductive films with an insulating film interposed therebetween,

wherein the gate electrodes of the vertical MISFETs respectively include a first film and a second film shaped in the form of sidewall spaces,

wherein the metal film is opened in a self-alignment with the first film, and

wherein the second film is electrically connected to the corresponding conductive film.

74. (Previously Presented) A semiconductor memory device comprising:

a memory cell provided with a first drive MISFET and a second drive MISFET and a first vertical MISFET and a second vertical MISFET,

wherein the drive MISFETs are formed on a major surface of a semiconductor substrate,

wherein a metal film is formed over the drive MISFETs with an insulating film interposed therebetween,

wherein the vertical MISFETs are formed over the metal film, and

wherein the metal film includes a tungsten film, and the first and second vertical MISFETs and the tungsten film are respectively electrically connected via a barrier film.

75. (Previously Presented) A semiconductor memory device comprising:

a memory cell which includes a first drive MISFET and a second drive MISFET and a first vertical MISFET and a second vertical MISFET, the first drive MISFET and the first vertical MISFET, and the second drive MISFET and the second vertical MISFET being cross-connected,

wherein the drive MISFETs are formed on a major surface of a semiconductor substrate,

wherein a metal film for cross-connecting gates and drains of the first and second drive MISFETs is formed over the drive MISFETs with an insulating film interposed therebetween,

wherein the vertical MISFETs connected to the metal film are formed over the metal film, and

wherein the metal film includes a tungsten film, and the first and second vertical MISFETs and the tungsten film are respectively electrically connected via a barrier film.

76. (Previously Presented) A semiconductor memory device comprising:

a memory cell which includes a first drive MISFET and a second drive MISFET and a first vertical MISFET and a second vertical MISFET, the first drive MISFET and the first vertical MISFET, and the second drive MISFET and the second vertical MISFET being cross-connected,

wherein the drive MISFETs are formed on a major surface of a semiconductor substrate,

wherein gates of the vertical MISFETs formed over the drive MISFETs with an insulating film interposed therebetween are electrically connected to lower conductive films at lower portions thereof and thereby electrically connected to gates or drains of the drive MISFETs, and

wherein the conductive film includes a tungsten film, and the first and second vertical MISFETs and the tungsten film are respectively electrically connected via a barrier film.

77. (Previously Presented) A semiconductor memory device comprising:

a memory cell which includes a first drive MISFET and a second drive MISFET and a first vertical MISFET and a second vertical MISFET, the first drive MISFET and the first vertical MISFET, and the second drive MISFET and the second vertical MISFET being cross-connected,

wherein the drive MISFETs are formed on a major surface of a semiconductor substrate,

wherein the vertical MISFETs are respectively formed over the drive MISFETs with an insulating film interposed therebetween,

wherein current paths between gates or drains of the drive MISFETs and gates of the vertical MISFETs are formed via lower portions of the gates of the vertical MISFETs through conductive films, and

wherein the conductive film includes a tungsten film, and the first and second vertical MISFETs and the tungsten film are respectively electrically connected via a barrier film.

78. (Previously Presented) A semiconductor memory device comprising:

a memory cell which includes a first drive MISFET and a second drive MISFET and a first vertical MISFET and a second vertical MISFET, the first drive MISFET and the first vertical MISFET, and the second drive MISFET and the second vertical MISFET being cross-connected,

wherein the drive MISFETs are formed on a major surface of a semiconductor substrate,

wherein conductive films electrically connected to gates or drains of the drive MISFETs are respectively formed over the drive MISFETs with an insulating film interposed therebetween,

wherein the vertical MISFETs are formed over the conductive films,

wherein gate electrodes of the vertical MISFETs are shaped in the form of sidewall spacers and electrically connected to the conductive films, and

wherein the conductive film includes a tungsten film, and the first and second vertical MISFETs and the tungsten film are respectively electrically connected via a barrier film.

79. (Previously Presented) A semiconductor memory device comprising:

a memory cell which includes a first drive MISFET and a second drive MISFET and a first vertical MISFET and a second vertical MISFET, the first drive MISFET and the first vertical MISFET, and the second drive MISFET and the second vertical MISFET being cross-connected,

wherein the drive MISFETs are formed on a major surface of a semiconductor substrate,

wherein conductive films electrically connected to gate electrodes or drains of the drive MISFETs are formed over the drive MISFETs with an insulating film interposed therebetween,

wherein the vertical MISFETs are formed over the conductive films, and

wherein gate electrodes of the vertical MISFETs are electrically connected to the conductive films in a self-alignment manner.

80. (Previously Presented) A semiconductor memory device comprising:

a memory cell with a first drive MISFET and a second drive MISFET, a first

transfer MISFET and a second transfer MISFET and a first vertical MISFET and a second vertical MISFET,

wherein the drive MISFETs and the transfer MISFETs are formed on a major surface of a semiconductor substrate,

wherein a metal film is formed over the drive MISFETs and the transfer MISFETs with an insulating film interposed therebetween, and

wherein the vertical MISFETs are formed over the metal film.

81. (Previously Presented) A semiconductor memory device comprising:

a memory cell including a first drive MISFET and a second drive MISFET, a first transfer MISFET and a second transfer MISFET and a first vertical MISFET and a second vertical MISFET,

the first drive MISFET and the first vertical MISFET, and the second drive MISFET and the second vertical MISFET being cross-connected,

wherein the drive MISFETs and the transfer MISFETs are formed on a major surface of a semiconductor substrate,

wherein a metal film for cross-connecting gates and drains of the first and second drive MISFETs is formed over the drive MISFETs and the transfer MISFETs with an insulating film interposed therebetween, and

wherein the vertical MISFETs connected to the metal film are formed over the metal film.

82. (Previously Presented) A semiconductor memory device comprising:

a memory cell including a first drive MISFET and a second drive MISFET, a first transfer MISFET and a second transfer MISFET and a first vertical MISFET and a second vertical MISFET,

the first drive MISFET and the first vertical MISFET, and the second drive MISFET and the second vertical MISFET being cross-connected,

wherein the drive MISFETs and the transfer MISFETs are formed on a major surface of a semiconductor substrate, and

wherein gates of the vertical MISFETs formed over the drive MISFETs with an insulating film interposed therebetween are electrically connected to lower conductive films at lower portions thereof and electrically connected to gates or drains of the drive MISFETs.

83. (Previously Presented) A semiconductor memory device comprising:

a memory cell including a first drive MISFET and a second drive MISFET, a first transfer MISFET and a second transfer MISFET and a first vertical MISFET And a second vertical MISFET,

the first drive MISFET and the first vertical MISFET, and the second drive MISFET and the second vertical MISFET being cross-connected,

wherein the drive MISFETs and the transfer MISFETs are formed on a major surface of a semiconductor substrate,

wherein the vertical MISFETs are respectively formed over the drive MISFETs with an insulating film interposed therebetween, and

wherein current paths between gates or drains of the drive MISFETs and gates of the vertical MISFETs are formed via lower portions of the gates of the vertical MISFETs through conductive films.

84. (Previously Presented) A semiconductor memory device comprising:

a memory cell including a first drive MISFET and a second drive MISFET, a first transfer MISFET and a second transfer MISFET and a first vertical MISFET and a second vertical MISFET,

the first drive MISFET and the first vertical MISFET, and the second drive MISFET and the second vertical MISFET being cross-connected,

wherein conductive films electrically connected to gates or drains of the drive MISFETs are formed over the drive MISFETs with an insulating film interposed therebetween,

wherein the vertical MISFETs are formed over the conductive films, and

wherein gate electrodes of the vertical MISFETs are shaped in the form of sidewall spacers and electrically connected to the conductive films.

85. (Previously Presented) A semiconductor memory device comprising:

a memory cell including a first drive MISFET and a second drive MISFET, a first transfer MISFET and a second transfer MISFET and a first vertical MISFET and a second vertical MISFET,

the first drive MISFET and the first vertical drive MISFET, and the second drive MISFET and the second vertical MISFET being cross-connected,

wherein the drive MISFETs and the transfer MISFETs are formed on a major surface of a semiconductor substrate,

wherein conductive films electrically connected to gates or drains of the drive MISFETs are formed over the drive MISFETs with an insulating film interposed therebetween,

wherein the vertical MISFETs are formed over the conductive films, and

wherein gate electrodes of the vertical MISFETs are electrically connected to the conductive films in a self-alignment manner.

86. (Previously Presented) A semiconductor memory device comprising:

a memory cell with a first drive MISFET and a second drive MISFET, a first transfer MISFET and a second transfer MISFET and a first load MISFET and a second load MISFET,

the drive MISFETs and the transfer MISFETs formed on a major surface of a semiconductor substrate such that a gate electrode of the first driver MISFET and a gate electrode of the first transfer MISFET extend over a first active region and such that a gate electrode of the second driver MISFET and a gate electrode of the second transfer MISFET extend over a second active region,

wherein the first active region extends in a first direction such that the gate electrode of the first driver MISFET and the gate electrode of the first transfer MISFET are arranged in the first direction and such that a gate length direction thereof is in parallel with the first direction,

wherein the second active region extends in the first direction such that the gate electrode of the second driver MISFET and the gate electrode of the second transfer MISFET are arranged in the first direction and such that a gate length direction thereof is in parallel with the first direction,

wherein the first driver MISFET and the second transfer MISFET are arranged in a second direction crossing to the first direction,

wherein the first transfer MISFET and the second drive MISFET are arranged in the second direction, and

wherein the load MISFETs are formed over the drive MISFETs and the transfer MISFETs with an insulating film interposed therebetween.

87. (Previously Presented) A semiconductor memory device according to claim 86, wherein the gate electrode of the first drive MISFET is arranged, in the second direction, in aligned with the gate electrode of the second transfer MISFET, and

wherein the gate electrode of the first transfer MISFET is arranged, in the second direction, in aligned with the gate electrode of the second drive MISFET.

88. (Previously Presented) A semiconductor memory device according to claim 87, wherein the first active region and the second active region are formed in a p well region,

wherein the transfer MISFETs and the drive MISFETs are n channel MISFETs, and

wherein the load MISFETs are p channel MISFETs.

89. (Previously Presented) A semiconductor memory device according to claim 87, wherein the load MISFETs are vertical MISFETs.

90. (Previously Presented) A semiconductor memory device according to claim 86, wherein the first active region and the second active region are formed in a p well region,

wherein the transfer MISFETs and the drive MISFETs are n channel MISFETs, and

wherein the load MISFETs are p channel MISFETs.

91. (Previously Presented) A semiconductor memory device according to claim 86, wherein the load MISFETs are vertical MISFETs.

92. (Previously Presented) A semiconductor memory device according to claim 80,

wherein a barrier metal layer is formed over the metal film, and

wherein each of the vertical MISFETs is formed over the barrier metal film and is electrically connected to the metal film via the barrier metal film.

93. (Previously Presented) A semiconductor memory device according to claim 92,

wherein the barrier metal layer is comprised of a TiN film, and

wherein the metal layer is comprised of a W film.

94. (Previously Presented) A semiconductor memory device according to claim 92,

wherein each of the vertical MISFETs is electrically connected to the metal film via a throughhole such that the throughhole is formed inside of the barrier metal film.

95. (Previously Presented) A semiconductor memory device comprising:

a first MISFET and a vertical MISFET,

wherein the first MISFET is formed on a major surface of a semiconductor substrate,

wherein a metal film is formed over the first MISFETs with an insulating film interposed therebetween,

wherein the vertical MISFET is formed over the metal film,

wherein a barrier metal layer is formed over the metal film, and

wherein the vertical MISFET is formed over the barrier metal film and is electrically connected to the metal film via the barrier metal film.

96. (Previously Presented) A semiconductor memory device according to claim 95,

wherein the barrier metal layer is comprised of a TiN film, and

wherein the metal layer is comprised of a W film.

97. (Previously Presented) A semiconductor memory device according to claim 95,

wherein the vertical MISFET is electrically connected to the metal film via a throughhole such that the throughhole is formed inside of the barrier metal film.